Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.081”**

**PAD FUNCTIONS:**

1. **OFFSET TRIM**
2. **– IN**
3. **+ IN**
4. **– VS**
5. **OFFSET TRIM**
6. **OUTPUT**
7. **+ VS**
8. **SUBSTRATE**

**1**

**2**

**3**

**4**

**8**

**7**

**6**

**5**

**627**

**MASK**

**REF**

**.119”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 X .004” min.**

**Backside Potential: FLOAT**

**Mask Ref: 627**

**APPROVED BY: DK DIE SIZE .081” X .119” DATE: 3/15/23**

**MFG: TEXAS/ BURR BROWN THICKNESS .011” P/N: OPA627**

**DG 10.1.2**

#### Rev B, 7/1